Reaching 1 Watt Reliable Output Power on Single-Mode 980 nm Pump Lasers

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ABSTRACT

Single-mode 980 nm pump lasers are mature products needed in an increasing range of applications and their power level has been constantly raised in the last fifteen years from a few tens of mW for the first generations of devices up to the current maximum level of 750 mW fiber-coupled output power. As the fiber output power increases, new applications provide positive feed-back to continue the development of these devices, although severe constraints are imposed both by reliability and the need for wavelength stabilization, which is generally built on the utilization of Fiber Bragg Gratings (FBGs). We have developed in 2005 a record saturation power device [1] (P_{sat}=2.35W @ 25 °C, for 3.9 mm cavity lengths) whose fiber-coupled power has reached 750 mW for 25 °C cooled applications, limited mainly by reliability as wavelength stabilization was already demonstrated up to levels above 1 Watt. 3S PHOTONICS has now developed a new generation of powerful and reliable devices that allow foreseeing operation at or close to 1W for cooled applications. We have further optimized the vertical structure to reduce the internal losses, and to reduce the junction temperature for increased reliability. High kink-currents around 2.5 A have been measured on the best devices. The gain bandwidth has been engineered to allow maintaining the wavelength stabilization even on very long laser cavities. Encouraging preliminary reliability results have also been obtained.

Keywords: Semiconductor, laser diode, GaAs, high-power, pump laser, single-mode, 980 nm.

1. INTRODUCTION

High power single-mode 980 nm pump lasers have been developed for almost 20 years now and it is legitimate to ask if the improvement of their intrinsic performance is still of interest or not. Remarkable performance levels have been reached in the last few years and the current state-of-the-art, maximum fiber output power level is currently in the range 0.6-0.75 W [1-4]. Different device architectures such as Tapered Lasers (TL) [5] or Slab-Coupled Optical Waveguide Lasers (SCOWL) [6] are able to provide higher single-lateral-mode powers but still lack the linearity, effective wavelength stabilization, reliability level and simple optical coupling and packaging schemes that are achievable using high power single-mode diode lasers. In addition, the input electrical power budget for these more complex devices is intrinsically much higher, limiting their utilization to applications where the large waste heat can be managed. As we will show in this paper, the margin for increased performance of the conventional Fabry-Perot single-mode pump lasers is still significant, provided that the vertical structure is engineered and optimized to guarantee full compliance with all the usual specifications. Basically, the performance improvement is based on the chip length scaling approach, which leads to the challenge of further lowering the (already low) internal loss level, so that the external efficiency can be kept constant on longer chips (for chip lengths L > 5mm) [7]. 3S PHOTONICS has developed a new generation of 980 nm single-mode pump lasers that allow operation at or close to 1 Watt, depending on the exact

reliability level required for each specific application. The total power budget needed to provide 0.8-1.0 W fiber output power is kept low by the reduced electrical and thermal resistances obtained on very long chips. Severe additional design requirements, though, are added by the need to stabilize the wavelength of the chip [7, 8], generally using Fiber Bragg Gratings (FBGs), and by the high reliability levels required by most applications [7, 9]. The new performance standard reached with the new generation of devices, which can be extended to the whole 920 – 1060 nm wavelength range [10], will allow significant improvements in Fiber Lasers (FLs), Frequency Doubling (FD) diode-based systems and other applications requiring fiber powers in the Watt range.

2. DEVICE TECHNOLOGY

The chip technology has been described in some detail in previous papers [1,11], and here we will give only a brief overview. The chip is based on a low-loss, asymmetric waveguide, vertical structure [7], while the lateral waveguide is provided by a conventional ridge waveguide, dry-etched using an Inductively Coupled Plasma reactor on full 3" wafers [11]. The ridge waveguide is longitudinally flared, and we have optimized the design of the flared ridge for improved performance. The injected current density is slightly reduced by a small increase in the injected area, with respect to previous lateral waveguide designs, when compared at constant cavity length. All the other steps in the chip fabrication process have not been modified and details are available in previous papers.

3. INTERNAL LOSS: ASSESSMENT and DISCUSSION

While optimizing a vertical structure is intrinsically a multi-parameter problem, the importance of the internal loss can hardly be overestimated [7, 12]. Most current, state-of-the-art, vertical structures designed for single-lateral-mode high power diodes already provide waveguides with losses below 1 cm^{-1}, but the lowest loss levels, around 0.3-0.4 cm^{-1}, are generally reached on multi-mode structures, due to less severe design constraints. The absence of need to finely control the strength of the lateral waveguide is probably the most important constraint removed, when designing a broad-area structure. Our previous generation of high-power single-lateral-mode 980 nm diode lasers was based on a vertical structure characterized by an internal loss level of 0.85 ± 0.10 cm^{-1} [1], that allowed the chip to reach record saturation powers around 2.5 W @ 25°C for a cavity length of 4.5 mm. These chips, with a cavity length of 3.9 mm, are currently packaged in butterfly cases and provide up to 0.75 W kink-free fiber output power, with a minimum nominal operating power of 0.68 W at a maximum injection current of 1.05 A @ 25°C (see the related Product Datasheet in [13]). In this Peltier-cooled configuration, their maximum output power is limited by the required, telecom-grade, reliability level, as the linear power exceeds the 0.75 W limit and can be as high as 1 W. The question then arises, if packaged diodes with a *reliable* fiber output power level of 1W can be designed and manufactured. To make them reliable, we need to lower both the junction temperature and the injection current density at the desired fiber output power level, which makes explicit the interest for longer cavities.

Longer chips, though, show degraded external efficiency, since this parameter (inversely) depends on the ratio of the internal to the mirror losses, and this ratio is quickly increased for longer chips. So, to keep the external efficiency constant at constant mirror reflectivities, the internal loss must be reduced by the same relative factor by which the length is increased, so as to keep the length-loss product also constant. Assuming that a 30% increase in device length is already an interesting target (namely a 5 mm device, assuming 3.9 mm as the reference), we can easily calculate that internal losses lower than 0.6 cm^{-1} are needed to get the same external efficiency on 5 mm devices.

Internal losses have been steadily reduced during the last decade, and Figure 1 shows the path followed at 3S PHOTONICS to reach a figure of 0.85 cm^{-1} in early 2005, and our current results. The mechanisms contributing to the internal losses are quite well-known, but their exact relative weights are more difficult to measure or calculate precisely [7]. Free Carrier Absorption (FCA), light scattering and Quantum-Well (QW) losses are often cited as the main mechanisms contributing to the residual loss figure, though there is no agreement in literature about their relative weight [14, 15]. This lack of agreement is, likely, simply due to the different vertical structures and non-uniform chip technologies.

The determination of the exact loss in our new vertical structure using the conventional method of the linear regression of the reciprocal external efficiencies versus cavity lengths proved to be relatively difficult. This is likely related to the fact that in very low loss structures the conventional method comes close to its accuracy limit, itself set by the unavoidable noise level in the determination of the slope efficiencies for different cavity lengths. An example of a

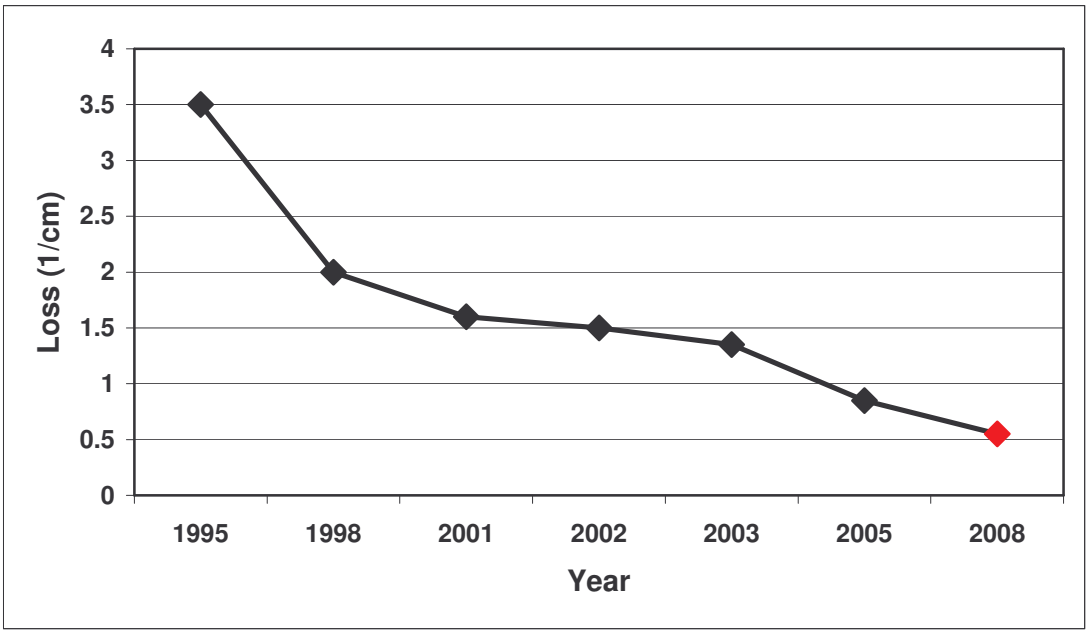

Fig. 1: Chronological evolution of the reduction of the internal losses at 3S PHOTONICS (1995-2008)

typical regression is shown in Figure 2. The internal losses calculated by the conventional method were found in the range 0.55-0.75 cm^{-1}, depending on the exact cavity lengths range used. Eliminating the shortest cavity length generally resulted in a lower figure for the loss, in the range 0.55 – 0.65 cm^{-1}. By measuring the Slope Efficiencies (SE) of coated devices, though, we had strong indirect evidence that the losses had been sensitively reduced. Indeed, at constant facet reflectivities, we observed, for 5.5 mm long cavities, SE figures equivalent to those routinely recorded on 3.9 mm chips with the previous vertical structure. The SE distributions for these coated devices are compared in Figure 3. Starting from the 0.85 cm^{-1} figure for the 2005 vertical structure, at constant facet reflectivities and slope efficiencies, a value between 0.55 and 0.60 cm^{-1} is extracted for the new vertical structure, which represents a substantial 30% reduction in the total waveguide loss. This value is also consistent with the range extracted from the conventional method applied in the 3.3 – 5.3 mm cavity length range.

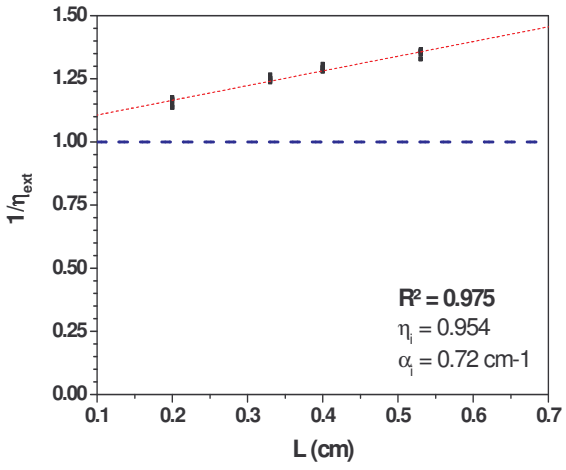

Fig. 2: Typical regression plot for internal loss assessment on the new generation chip

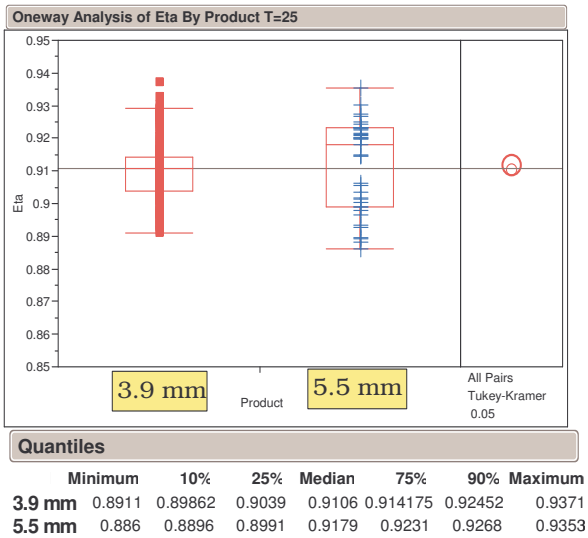

Fig. 3: SE comparison for 3.9 mm devices (previous structure) and 5.5 mm devices (new structure)

Also, the vertical structure has been optimized with respect to its electrical properties, resulting in a series resistance lowered by an additional 20% compared to the expected reduction due to the increased chip length, thus allowing to further reduce the junction temperature at high injection currents.

4. CHIP-on-SUBMOUNT RESULTS

4.1 – Electro/Optical Parameters and Junction Temperatures

The typical Light-current (LI) curves for the new structure, 5.5 mm long chips, in the 0 – 2 A current range at a heat-sink temperature of 25 °C are shown in Figure 4 (3 devices at each temperature). It can be observed that the linear power exceeds 1.5 W @ 2 A. This power level is, in itself, closely comparable to what was obtained on 3.9 mm chips [1], again proving that the internal loss has been lowered enough to completely preserve the power performance on much longer devices. The kink-free current for the new devices exceeds 2 A, and kinks are generally detected slightly above 2.3 A. However, the structures have not been fully optimized yet with respect to the strength of the lateral waveguide and we believe that a precise optimization of the index step could improve the kink level by several hundreds mA. Threshold currents are in the range 75 to 95 mA depending on the exact facet reflectivity on each diode, and the median SE value is around 0.92 W/A. The series resistance median value is 0.19 Ohm. The driving voltage is well below 2 V even at 2 A, and is as low as 1.65 V at 1.5 A. Also shown in Fig. 4 are the LI curves at 75 °C. Power levels around 1.0 W are reached at 1.5 A / 75°C. It is worth noting that in the low current range (I_{th} to 0.3 A) the Slope Efficiency is reduced by only 5% at 75 °C with respect to its value at 25°C (see inset of Fig.4).

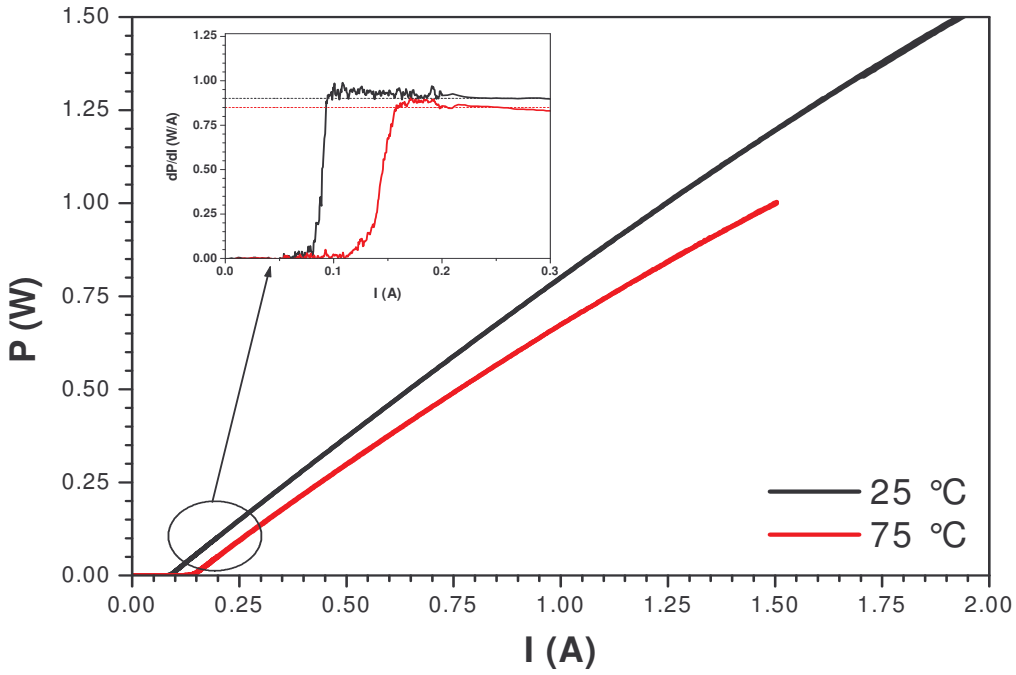

Fig. 4: LIV curves for 3 x 5.5 mm long chips @ 25 and 75 °C. Curves for the 3 devices are superposed at both temperatures. Inset: dP/dI curves at 25 and 75°C.

The most important feature of the new devices is related to the strong reduction of both the junction temperature and the injection current density for a given operation current [7]. In Fig.5 we compare the junction temperature, extracted from LIV measurements, of 3.9 mm long chips adopting the previous vertical structure, with 6.0 and 7.5 mm long chips built with the optimized vertical structure. It can be observed that, setting the junction temperature of the 3.9 mm chip at its highest telecom-grade reliable operation current as a reference (32.7 °C @ 1.05 A), the new chips would extend the operation current range by 52% (6.0 mm chips, to 1.60 A) or even 75% (7.5 mm chips, to 1.85 A), without exceeding the reference junction temperature. We will see that the chip power penalty is, as expected, almost completely reduced to zero for 6.0 mm chips, due to the reduction of the internal losses. For the longest chips, an injection current penalty at the same fiber output power exists, but we will show in a later section, devoted to results obtained on packaged devices, that it is remarkably small.

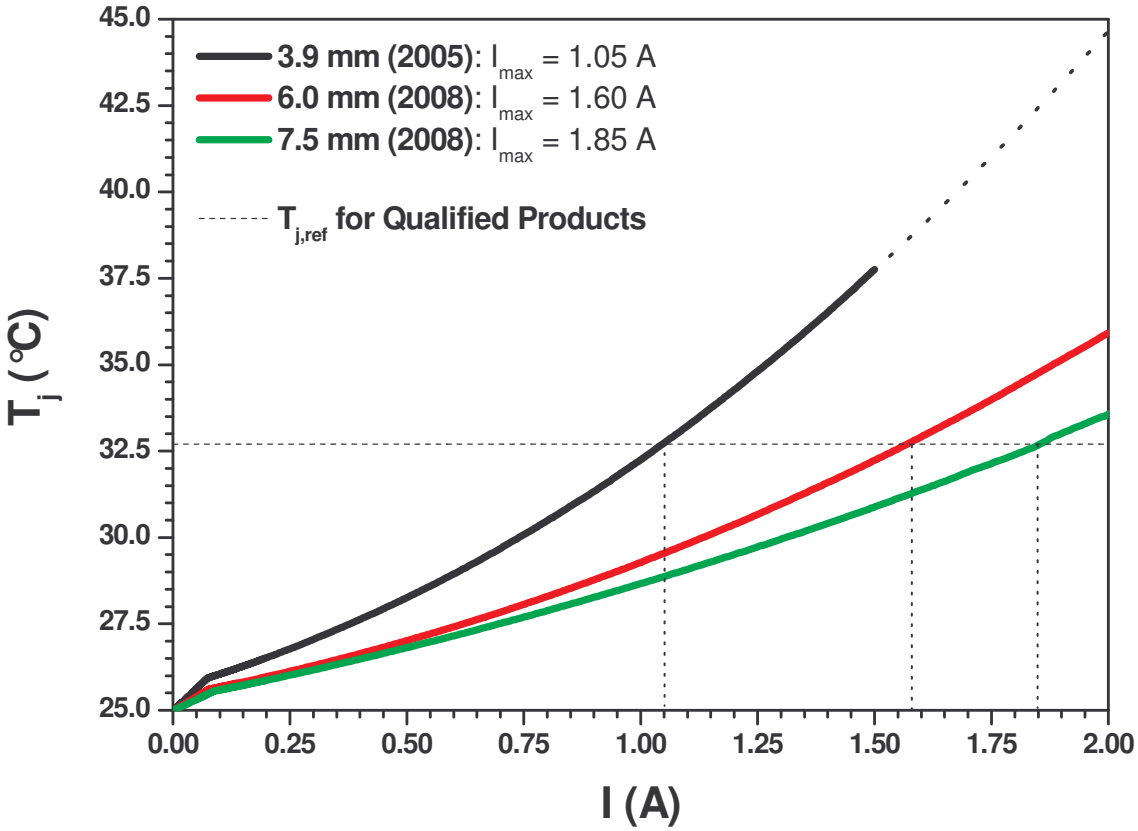

Fig. 5: Comparison of the junction temperature increase with injection current for new generation chips of different lengths and the standard 3.9 mm chip developed in 2005

4.2 – Beam Properties

Ridge waveguide lasers are designed for single-lateral mode operation, but the lateral waveguide characteristics slowly evolve towards multi-lateral mode behavior as the injection current is increased. This is due both to thermal effects and to other carrier effects that modify the lateral refractive index profile, guiding the optical mode in the horizontal direction. Figures 6 and 7 show that the inevitable transition to multi-lateral mode operation is rejected to currents above 2.25 A for 5.5 mm devices. In Fig. 6, the lateral Far-Field (FF) pattern is shown at different currents up to 2.5 A. It can be noted that

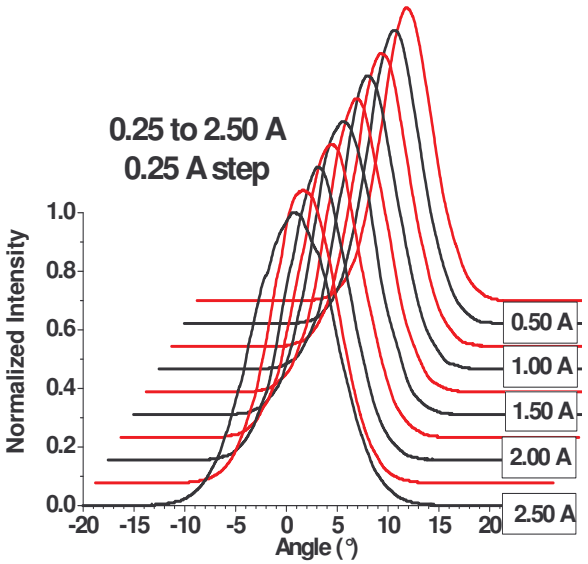

Fig.6: Lateral Far-Field profiles in the 0.25-2.50 current range

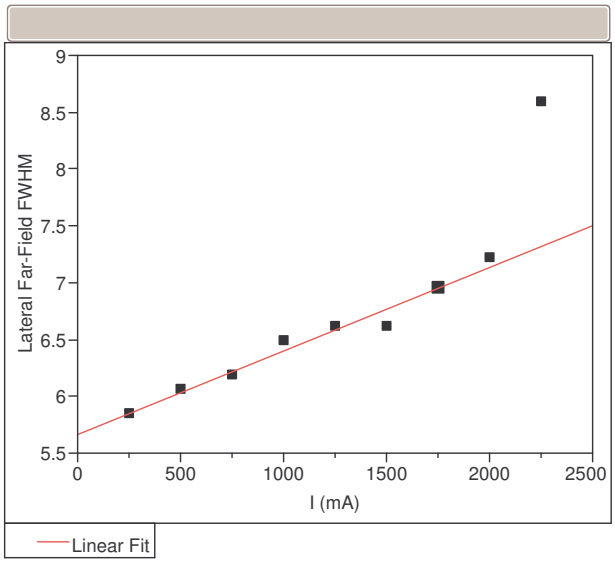

Fig.7: FWHM as a function of the injection current extracted from the profiles shown in Fig. 6

the mode profile stays in the fundamental mode up to 2.25 A and that shoulders due to the first order mode are only observed at 2.5 A. In Fig.7, additionally, the Full Width at Half Maximum of the lateral FF profile is plotted versus injection current and it can be seen that it linearly increase up to 2.25 A and only at 2.5 A sudden widening occurs, which confirms the onset of the first-order mode. Finally, Fig.8 shows the angular stability of the lateral beam direction: the angular position of the centroid of the Gaussian fit to the lateral FF profile is plotted vs. injection current, and it is easily observed that no beam steering occurs in the whole single-lateral mode current range (up to > 2.0 A). The maximum angular deviation of the beam measured on a large set of 5.5 mm devices did not exceed 0.32° for currents up to 1.75 A. The distribution of the angular deviations is shown in Fig.9. The stability of the beam will be further indirectly confirmed by the results obtained on packaged devices that are the subject of a following section.

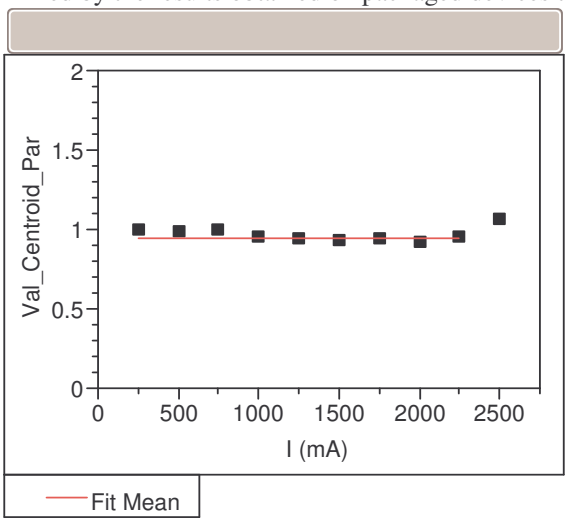

Fig.8: Angular position of the lateral Far-Field Gaussian fit centroid as a function of the injected current

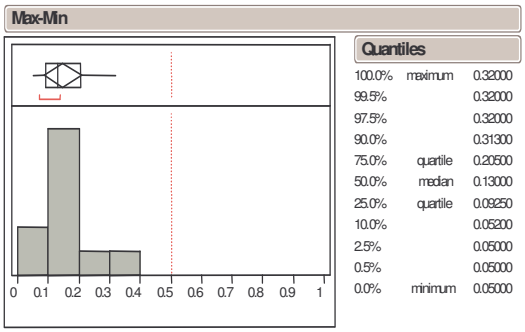

Fig.9: Distribution of the Maximum angular deviation of the lateral FF centroid in the 0 – 1.75 A current range

4.3 – Preliminary Robustness and Reliability Results

The intrinsic robustness of the vertical laser structure and of the whole device is demonstrated by measurements of the roll-over power with injected currents as high as 4 A, which is the limit of our equipment. In fact, it is easily observed from Fig. 10 that even at 4 A the power-current characteristic curve does not saturate for devices with cavities of 6 mm or longer. The output power of a 6.0 mm diode at 4 A is as high as 2.8 W and we believe that, for both 6.0 and 7.5 mm chips, the roll-over power would exceed 3.0 W, injecting currents in the 4 – 5 A range.

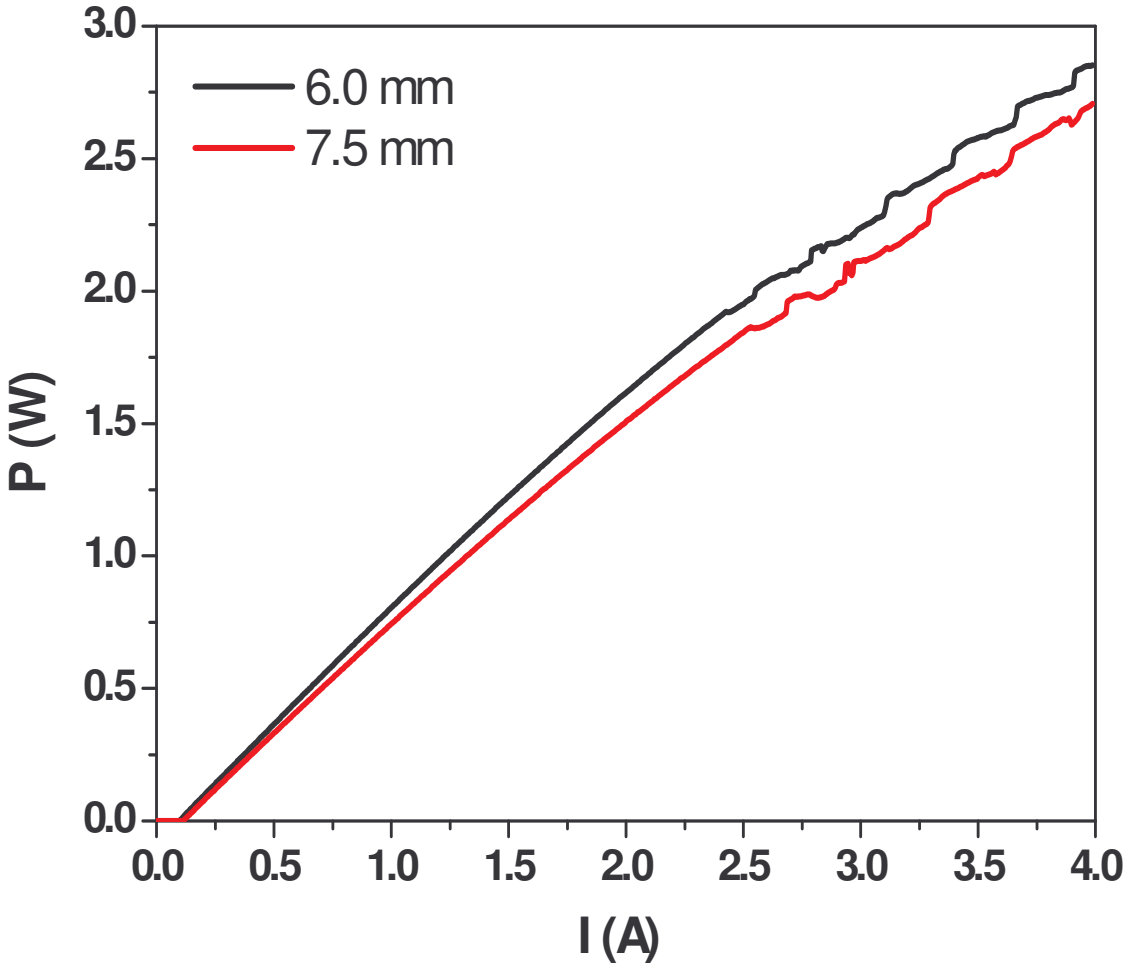

Fig. 10: LI curves up to a maximum current of 4.0 A for 6.0 and 7.5 mm chips

The new devices have also been tested at very high injection currents (1.2 – 1.6A) and high heat-sink temperatures (70-110 °C), both during step-stress tests and Constant Current aging tests. The next figure (Fig.11) shows, as an example, the relative power variation during a step-stress test, at constant injection current (1.4 A), in which the temperature was automatically raised by 10 °C every 144 hrs. It must be emphasized that the sub-mount temperature is much higher than the oven temperature indicated in the figure, due to the thermal power dissipated by neighbor lasers and the overall thermal resistance of the fixture. We measured the sub-mount temperature at values 20 – 25 °C higher than the oven average temperature shown in the figure. Aging test on a large sample of devices are now being started so that the exact reliability levels can be quantified at the different operating conditions for chips of different lengths [16].

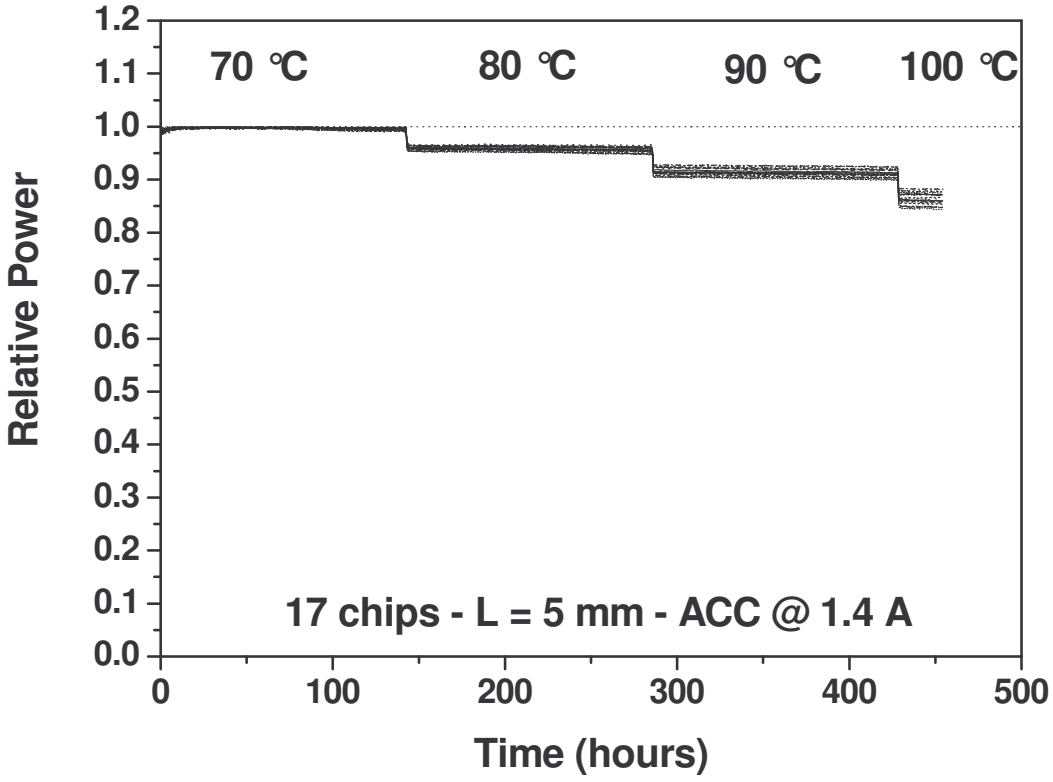

Fig. 11: Preliminary Step-stress tests on 5 mm devices at constant injection current (1.4 A) and temperature raised by 10°C every 144 hrs

5. RESULTS on PACKAGED DEVICES

The new devices have been packaged in Butterfly cases using a high performance coupling technology [17]. We used chips of 6.0 and 7.5 mm cavity lengths coupled to a Polarization Maintaining Fiber (PMF). The wavelength was stabilized using a Fiber Bragg Grating (FBG) with a reflectivity of a few percent. The packaged devices were measured at 25 °C and the LI curves for both cavity lengths are shown in Figure 12.

As it can be seen from Fig.12, the LI characteristic for the 6.0 mm long chip is quite close to its counterpart curve for the 3.9 mm device. This result is expected from the equivalent SEs recorded on 3.9 mm and 5.5 mm chips shown in Fig. 3. Even the output power level of the 7.5 mm packaged device is not strongly reduced with respect to the 3.9 mm chip reference. The injection current penalty does not exceed 150 mA for an output power of 1 W. In Fig. 12 we also show on the right scale axis the junction temperatures for the same devices, already discussed in §4.1 and shown in Fig.5. Clearly, with longer cavities, we can use much higher injection currents without exceeding the reference junction temperature in operation condition defined by the 3.9 mm chip at 1.05 A.

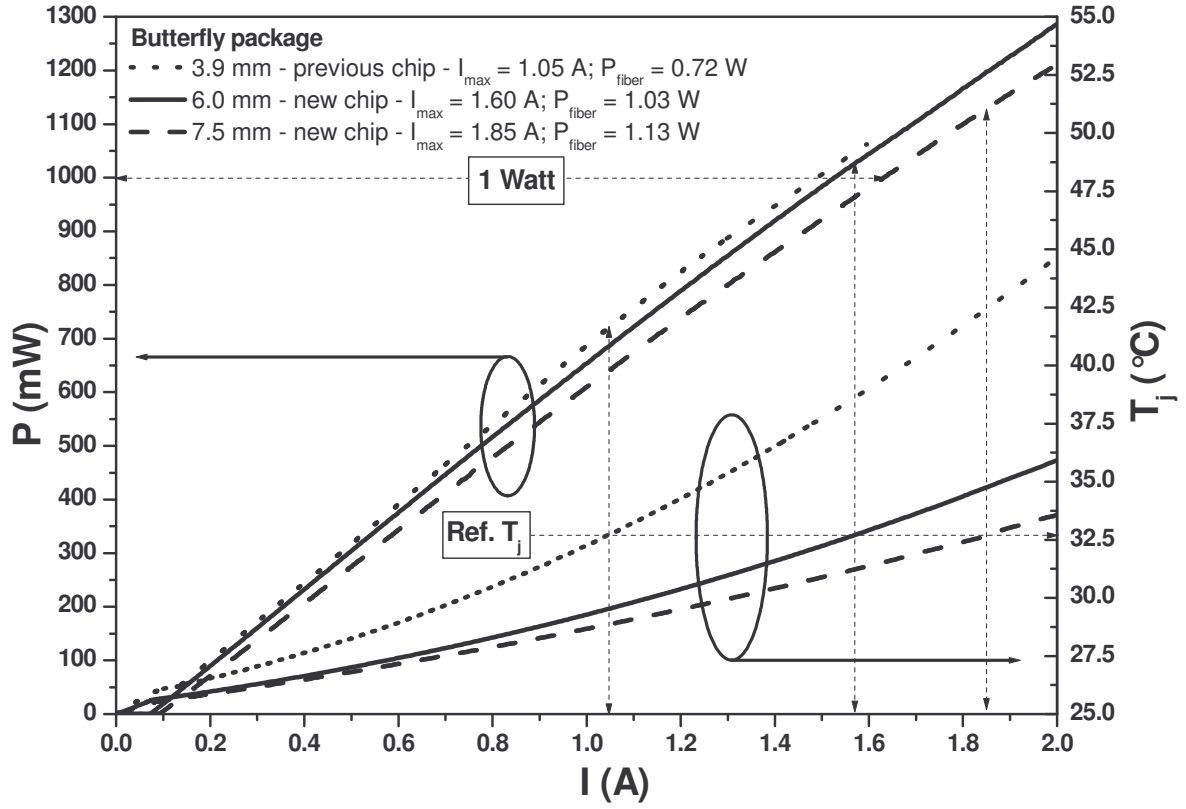

Fig. 12: LI curves for packaged new devices (6.0 and 7.5 mm long) compared to a 3.9 mm chip. The vertical arrows show the maximum injection currents/powers reached without exceeding $T_{j,ref}$

Table 1 summarizes the junction temperatures and the linear injection current densities of each chip for operation at 1 W. The linear injection density is used since the flared ridges have almost equivalent (within a few %) average widths for both generations of devices. The 6.0 mm chip is able to keep the junction temperature at the reference level and lower the injection density by 6%, while the 7.5 mm chip, even with a small injection current penalty, has the potential to reduce the junction temperature by 3-4% and the injection linear current density by nearly 20%. Remarkably, the substantial internal loss reduction obtained on the new vertical structure limits the injection current penalty to 10% of the operating current recorded for 3.9 mm chips, for a device that is almost doubled in length. These figures perfectly illustrate the large reliability potential of very long devices with cavities in the 5.0 - 7.5 mm range.

Chip	I @ 1W (A)	Ratio to I_{ref} -	T_j @ 1W (°C)	Ratio to $T_{j,ref}$ -	J_{inj} @ 1W (A/mm)	Ratio to $J_{inj,ref}$ -
3.9 mm (2005)	1.50	1.43	37.8	1.156	0.385	1.42
6.0 mm (2008)	1.53	1.46	32.5	0.994	0.255	0.94
7.5 mm (2008)	1.65	1.57	31.6	0.966	0.220	0.81

Table 1: Comparison of Operating currents, Junction Temperatures and linear Injection Densities at 1.0 W Fiber Output Power, at 25 °C, for Butterfly packaged devices.

Finally, we also show that the FBG wavelength stabilization properties have been maintained by properly engineering the gain spectrum. In Figure 13, the locking of the 6.0 mm chip (whose LI curve is shown in Figure 12) is demonstrated by the wavelength plotted as a function of the injected current (lower curve, right scale), and also by the excellent Gain Peak Suppression Ratio (GPSR) extracted from the spectra (upper curve, left scale). The GPSR is above 40-45 dB from 250 mA to 2.0 A. The insets in Fig.13 show the spectra recorded at 1.0 A (left inset) and 2.0 A (right inset) in the 960 — 1000 nm wavelength range. The strong suppression of the gain peak emission is fully confirmed by the spectra.

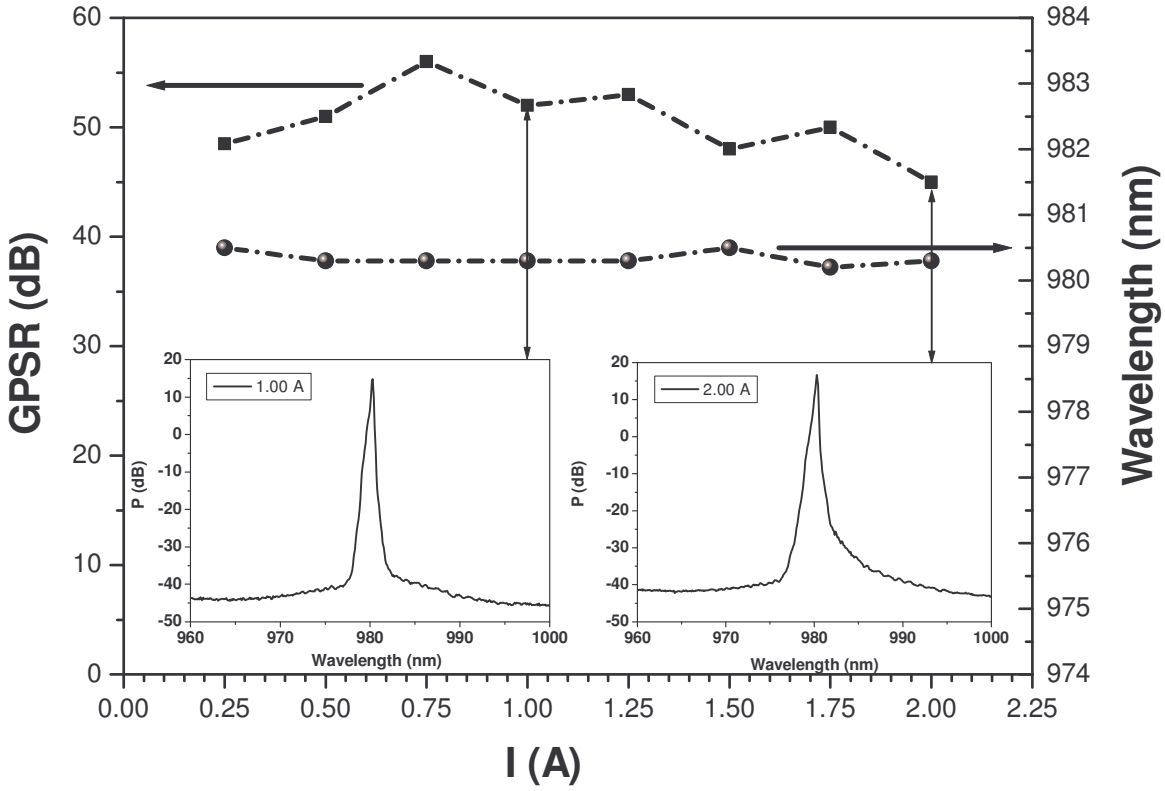

Fig.13: GPSR and wavelength as a function of current for a 6.0 mm device stabilized with an FBG at 980 nm in a Polarization Maintaining Fiber. Insets: Spectra recorded at 1.0 A (left) and 2.0 A (right).

6. CONCLUSIONS

We have developed a new generation of single-lateral-mode 980 nm high power devices based on a vertical structure with internal losses as low as 0.55 – 0.60 cm^{-1}. Devices with cavity lengths in the 5.0 – 7.5 mm range based on the new vertical structure can now bear the comparison with shorter devices in terms of external efficiency, but have the additional advantage of much lower junction temperatures and injection current densities. With the new devices, fiber output powers in the Watt range could be demonstrated, while also keeping the junction temperature and the injection current density in a safe range, defined using, as a reference, previously qualified products.

7. ACKNOWLEDGMENTS

We would like to thank J.Perinet and M.Biet for interesting discussions and J.P.Fie, P.Flohic, D.Cillierre, J.Peberge, M.Loon, D.Buterin, G.Quitte, K.Mekhazni, B.Girard, E. Rampazzi and P.Bourdeaux for excellent technical assistance during the whole project.

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