Tolerances and Receiver Sensitivity Penalties of Multibit Delay Differential-Phase Shift-Keying Demodulation

Yannick Keith Lizé, *Student Member, IEEE*, Louis Christen, *Student Member, IEEE*, Moshe Nazarathy, *Senior Member, IEEE*, Yuval Atzmon, Scott Nuccio, *Student Member, IEEE*, Poorya Saghari, *Student Member, IEEE*, Robert Gomma, Jeng-Yuan Yang, Raman Kashyap, *Member, IEEE*, Alan E. Willner, *Fellow, IEEE*, and Loukas Paraschis, *Member, IEEE*

***Abstract*—Multibit delay demodulation of differential-phase shift-keying (DPSK) is finding applications in polarization interleaved modulation, optical time-domain multiplexing (OTDM), and multisymbol DPSK demodulation. Little attention has been paid to the degradation in tolerance and power penalty associated with multibit delay demodulation. We assess experimentally, numerically, and analytically the power penalties and tolerances associated with multibit delay DPSK demodulation. Numerical and analytical results show that the power penalty scales by a small factor of 0.2–0.35 dB per integer bit delay due to laser linewidth (LW) while experimental back-to-back results show a significant 1.2 dB per integer bit delay due to frequency offset penalty of longer bit delays. Frequency offset tolerance scales as 1/bit-delay and the delay-mismatch tolerance decreases by 20% for delays longer than 1 bit. A simple analytic model accounts for the combined effect of LW, frequency offset, and amplified spontaneous emission.**

***Index Terms*—Delay lines, demodulation, differential phase shift keying (DPSK), frequency stability, optical time-domain multiplexing (OTDM), polarization interleaving.**

I. Introduction

DIFFERENTIAL-PHASE shift keying (DPSK) is currently under serious consideration as a deployable data-modulation format for high-capacity optical communication systems due to its high receiver sensitivity and tolerance to certain nonlinear effects. The typical binary DPSK [1] receiver uses a Mach-Zehnder delay-line interferometer (DLI) with balanced detection, and 1-bit delay in one arm, demodulating the differential phase between each data bit and its successor. There has been much recent interest in the concept of modified DLIs with multibit delay in one arm, demodulating the differential phase between successive data bits that are a fixed number of bit time slots apart. DPSK receivers equipped with such a function are used in the following applications. 1) Demodulating data streams that have been time-multiplexed using polarization interleaving, such that each bit is compared to a previous bit in the same polarization state [2], [3], which can mitigate certain nonlinear effects. 2) Demodulating an optically time-division-multiplexed (OTDM) data stream, such that each data bit is compared to a previous bit from the same transmitter [4]. This is also important in laboratory experiments when using a single transmitter, where the OTDM multiplexer does not provide phase stability. 3) a DPSK receiver using several DLIs of various bit delays, with the DLI outputs all combined using postprocessing, to achieve higher receiver sensitivity [5], [6]. Although DPSK demodulation has been extensively investigated [7]–[10], there has been little discussion on the actual system penalty incurred by multibit delay demodulation [11].

We present experimental results, and numerical and analytic analysis of the penalties associated with multibit DPSK demodulation due to frequency offset (FO) as described in Fig. 1, laser linewidth (LW), and the bit delay offset. Simulation results along with an simple analytic model indicate that the optical signal-to-noise ratio (OSNR) penalty associated with detection through multibit delay scales as 0.2–0.35 dB per integer bit delay at 10 Gb/s with a 10-MHz LW. We also find that the FO tolerance scales as the inverse of the bit delay. Furthermore, the bit delay mismatch penalty increases for 2-bit delay demodulation, but no further degradation occurs for longer delays. These key limitations may reduce the effectiveness of multibit delay methods in some applications.

II. Model and Experimental Setup

Over a realistic fiber optic link, it has been shown that the total linear and nonlinear phase noise has a nearly Gaussian distribution [12]. Extending the Gaussian approximation to laser-induced phase noise [13], a simple analytic model is derived for M-ary DPSK detection, with Q^2-factor of the total demodulated Gaussian noisy angle given by

$$Q^2 = (\pi/M - \gamma)^2 / \left(\sigma^2_{\mathrm{LN+NL}} + \sigma^2_{\mathrm{LPN}}\right) \qquad (1)$$

where $\gamma \equiv 2\pi\Delta\nu_c Td$ is the phase offset between the two DLI arms, with $\Delta\nu_c$ the frequency offset away from the optimal optical carrier, $\sigma^2_{\mathrm{LN+NL}}$ is the variance of the linear and nonlinear phase noise, and the laser phase noise (LPN) variance is given in the first perturbation order by the expression

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Y. K. Lizé, L. Christen, S. Nuccio, P. Saghari, J.-Y. Yang, and A. E. Willner are with the Viterbi School of Engineering, University of Southern California, Los Angeles, CA 90089–2565 USA (e-mail: ylize@itflabs.com).

M. Nazarathy and Y. Atzmon are with the Electrical Engineering Department, Technion, Israel Institute of Technology, Haifa 32000, Israel.

R. Gomma and R. Kashyap are with the Advanced Photonics Concepts Laboratory, École Polytechnique de Montréal, Montréal, QC 3010, Canada.

L. Paraschis is with Advanced Technology, Core Routing, Cisco Systems, San Jose, CA 95134 USA.

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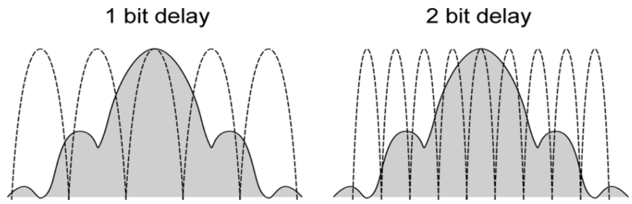

Fig. 1. Spectral response (dash curve) of a 1-bit (left) and 2-bit (right) delay delay-line interferometer overlayed on a DPSK spectrum. The narrower free-spectral range increases the frequency offset sensitivity.

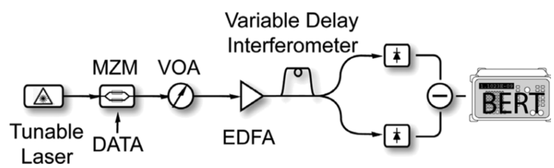

Fig. 2. Experimental setup to obtain receiver sensitivity and OSNR penalty measurements. Different bit delays are obtained through the variable delay interferometer.

$$\sigma^2_{\rm LPN} = 2\pi\Delta\nu_{\rm LW}T(d-1/3) \tag{2}$$

with $\Delta\nu_{\rm LW}$ the full-width at half-maximum (FWHM) laser LW, T^{-1} the bit rate, and d the integer number of bit delays. The OSNR penalty in decibel units is readily extracted from (1) and (2) with its functional dependence due to the combined effect of LW, FO, and multibit bit delays

$$-10\log_{10}[1-2M\Delta\nu_c Td]+10\log_{10}\left[1+\frac{2\pi\Delta\nu_{\rm LW}T\left(d-\frac{1}{3}\right)}{\sigma^2_{\rm LN+NL}}\right]. \tag{3}$$

The value of $\sigma^2_{\rm LN+NL}$ in Figs. 3 and 4 further below was set such that for zero LW and FO penalties the linear phase noise induces a BER of 10^{-9} while the nonlinear phase noise power is zero.

For our experimental results, we constructed a stable delay interferometer with tunable delay providing an FSR ranging from 3.2 to 11 GHz. Two 3-dB fiber couplers were spliced together; one branch wound onto a fixed wheel and the other branch wound on two half wheels with tunable separation, stretching the fiber to provide the variable time delay. The extinction ratio exceeded 15 dB and BER was measured for a 10-Gb/s signal using the setup of Fig. 2.

Simulations were performed for a 10-Gb/s RZ-DPSK signal on a 10-MHz LW laser using 12.5-GHz third-order Gaussian optical filtering and 8-GHz Lorentzian electrical filtering at the receiver. A Karhunen–Loeve expansion for non-Gaussian noise statistics was used with 512 bits simulated at 64 samples per bit. Complete BER versus OSNR curves were simulated and the OSNR penalty at BER $= 10^{-9}$ was inferred from those curves through a linear fit of the log (log(BER)) curve.

III. Laser Linewidth Penalty

With the frequency offset set to zero in (2), the OSNR penalty versus laser LW is illustrated in Fig. 3. At 10-MHz LW and 10 Gb/s, the degradation is ~0.35 dB per bit delay. The penalty

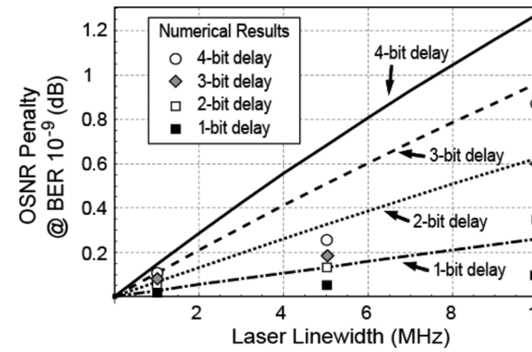

Fig. 3. Analytic (lines) and numerical (dots) results for the OSNR penalty versus laser LW for a 10-Gb/s signal for different bit delay $d = 1, 2, 3, 4$ in the interferometer.

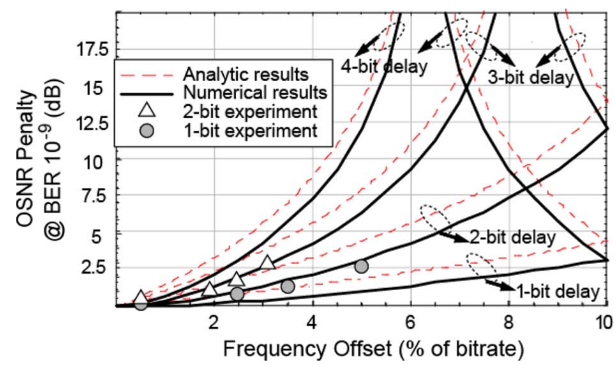

Fig. 4. Analytic, numerical, and experimental results for the OSNR penalty versus frequency offset for different bit delay. The simple analytic model approximates the experimental results while showing similar asymptotic trends of the numerical results.

is associated with the finite coherence time of the laser, or equivalently it is due to the random walk of the phase noise Wiener process, with its variance building up over the multibit delay. For fixed LW and bit delay, increasing the bit rate will decrease the penalty. Simulations show a penalty of 0.2 dB per bit delay at 10 MHz. Since linear phase noise is not exactly Gaussian and our results do not include nonlinear phase noise, there is a small discrepancy between analytic and numerical results.

IV. Frequency Offset Penalty

By setting the laser LW to zero in (2), the analytic penalty due to the frequency offset is as shown in Fig. 4, which also illustrates the simulated frequency offset penalty. The 1-bit delay numerical curve is similar to previously results for 1-bit delay frequency offset [10]. As expected, the frequency offset penalty scales as the inverse of the bit delay such that a 1-dB penalty is obtained for an offset comparable to 4% of the bit rate at 1-bit delay but that the same penalty occurs at 2%, 1.33%, and 1% for 2, 3, and 4 bit delay, as shown in Fig. 4. As expected, the penalty increases with increasing bit delay but decreases with increasing bit rate. Experimental results shown in Fig. 4 exhibit a similar trend as the numerical results, but were found to be more sensitive to frequency offset. Such discrepancy has been observed in other reported experimental results [8]–[10]. There is also a discrepancy between analytic and numerical results which can be explained by the Gaussian phase noise approximation. As

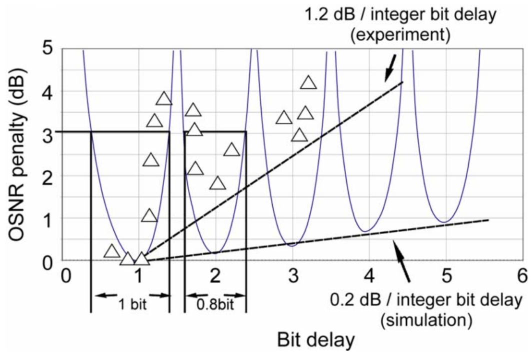

Fig. 5. OSNR penalty versus delay at BER 10^{-9}. Experimental results scale as 1.2 dB per integer bit delay due to frequency offset for longer delays while simulation show a 0.2 dB penalty due to laser LW. The delay mismatch penalty 3 dB range is 1 bit wide around 1-bit delay but only 0.8 bit at greater delays.

expected, both the simple analytic model and simulation results show the same asymptotic behavior versus offset and a decrease in penalty passed 25% of the FSR value. For negligible laser LW, the FO penalty is independent of the linear amplified spontaneous emission (ASE) and nonlinear phase noise (3). This can also be interpreted as independence of the optical filter bandwidth and shape, and was numerically validated.

V. Bit Delay Penalty

The OSNR penalty for multibit delay DPSK demodulation in back-to-back transmission is illustrated in Fig 5. We numerically determined a penalty for multibit delay scaling up with a slope of ~0.2 dB per integer bit delay which is in par with analytic and numerical results for laser LW penalty presented in Fig. 4. Experimentally, using a variable delay interferometer, we measured a greater penalty of 1.2 dB per integer bit delay as shown in Fig. 5. We also measured BER versus received power on a different experimental setup using three commercial demodulators with FSRs of 10, 5, and 2.5 GHz. A receiver sensitivity penalty of around ~1 dB/integer-bit-delay was again observed.

Our experimental penalty is significantly higher than in the numerical results and also exceeds the previously observed penalty using a 40-Gb/s DPSK signal in a 40-GHz and 10-GHz demodulator [14]. The excess experimental penalty is explained by the use of a tunable FSR demodulator and 5-GHz and 2.5-GHz demodulators that are not phase tunable, causing a frequency offset error due to imperfect alignment of the laser frequency to the transmission peak of the DLIs. Moreover, silica-based interferometers drift with about 1.5 GHz/°C, such that a small temperature change of ±0.1°C without active tuning will create a frequency offset of ±150 MHz. The offset is small for a 40-GHz or 10-GHz demodulator, but will create a significant penalty at 5 or 2.5 GHz.

The bit delay mismatch penalty has been widely investigated [9], [10]. Back-to-back bit delay mismatch penalty can be seen in Fig. 5. The results around 1-bit delay agree with previously reported results. Partial-bit delay mismatch (<1 bit) incurs a smaller penalty for the same percentage mismatch, since part of the bit interferes with itself, always yielding the same deterministic constructive interference. At multiple bit delays, the time mismatch translates partial interference with bit n and partial interference with bit $n+1$ which will yield different interference depending on the phase relationship between n and $n+1$. The result is that the 3-dB OSNR penalty *bandwidth* on FSR mismatch varies as 1/bit rate for 1-bit delay but tolerance is decreased to 0.8/bit rate for 2-bit delay or more, as illustrated in Fig. 5.

VI. Conclusion

The receiver sensitivity penalty associated with multibit delay DPSK demodulation was demonstrated numerically, experimentally, and analytically. The laser LW penalty was shown numerically and analytically to scale as ~0.2–0.35 dB per integer bit at 10 Gb/s for a 10-MHz LW. Experimental results show a 1.2-dB penalty per integer bit delay due to reduced frequency offset tolerances which reduce with 1/bit-delay. The delay-mismatch tolerance decreases by 20% for delays longer than one bit. Such limitations may need to be considered for polarization interleaved, OTDM, and multichip DPSK demodulation applications [1].

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